

## **A Novel Transformerless High Voltage Gain DC Converter Supplying Single Phase Full Bridge Inverter**

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**Abstract :** *In this paper, a novel transformerless high voltage gain dc converter supplying single phase full bridge inverter is proposed. The proposed topology contains a converter section and an inverter section. The converter utilizes input parallel output series configuration for providing a much higher voltage gain without adopting an extreme large duty cycle. The converter also reduces the voltage stress of both active switches and diodes and finally reduces both switching and conduction losses. The converter features automatic uniform current sharing without adding extra circuitry or complex control methods. Closed loop PI controller is used to control the error and achieves the desired output voltage for the converter section. The converter section is followed by a single phase full bridge inverter. The inverter uses unipolar switching technique. Inverter offers reduced switching losses and generates less EMI. The inverter with filter circuit gives better output sinusoidal voltage. The proposed topology applications may include UPS, power grid, renewable energy applications etc. The operation principle and steady state analysis of both converter and inverter sections are presented. Finally, some simulation and experimental results are presented to demonstrate the effectiveness of the proposed topology.*

**Keywords :** *Interleaved boost converter, PI controller, Voltage gain*

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### **I. INTRODUCTION**

With the shortage of the energy and ever increasing of the oil price, research on the renewable and green energy sources, especially the solar arrays and the fuel cells, becomes more and more important. How to achieve high step-up and high efficiency DC/DC converters is the major consideration in the renewable grid-connected power applications due to the low voltage of PV arrays and fuel cells. Environmental concerns about global warming, fossil fuel exhaustion, and the need to reduce carbon dioxide emissions provided the stimulus to seek renewable energy sources. Since the power density of a fuel cell is higher than other renewable energies, it can be widely used for grid-connected generation, vehicles, and portable applications. Generally, the fuel cell stack has a low voltage and its current ripple should be small. Therefore, a high step-up dc-dc converter with high voltage conversion ratio, low input-current ripple, and high efficiency is required. For the applications such as renewable energy, power grid, UPS an inverter is essential. There are many inverter topologies and inverter switching schemes and each one will have its own advantages and disadvantages. Efficiency and output distortion are two important factors governing the choice of inverter system.

In 2009 Wuhua Li et al presented a review paper of Non-Isolated High Step-Up DC/DC Converters in Renewable Energy Applications [2].The advantages and disadvantages of these converters are discussed and the major challenges of high step-up converters in renewable energy applications are summarized. An active clamp converter is introduced to provide higher voltage gain in 2009 [4]. The proposed system consists of an input-current doubler, an output-voltage doubler, and an active clamp circuit. The input-current doubler and the output-voltage doubler provide a much higher voltage conversion ratio without using a high turns ratio in the transformer and increase the overall efficiency. Moreover, the cost is increased because many extra power components and isolated sensors or feedback controllers are required. To make the PV generation system more flexible and expandable, the backstage power circuit is composed of a high step-up converter and a pulse width modulation (PWM) inverter [5].

The switched capacitor-based converters proposed in provide solutions to improve the conversion efficiency and achieve large voltage conversion ratio [6]. The use of the voltage multiplier technique applied to the classical non-isolated dc-dc converters in order to obtain high step-up static gain, reduction of the maximum switch voltage, zero current switching turn-on. Furthermore, many switched capacitor cells are required to obtain extremely high step-up conversion, which increases the circuit complexity. The energy-efficiency issue of switched-capacitor converters is still a controversial topic that requires a more in-depth discussion. In 2013 Chun-Kit Cheung et al presented a paper on Energy Efficiency of Switched Capacitor Converters [7]. In this paper, we address the issue by dividing the analysis of the entire efficiency problem into two parts. In the first part, the efficiency of a capacitor-charging RC circuit under different aspects (partial charging, full charging, at

zero capacitor voltage, at nonzero capacitor voltage, etc.) will be conducted. Several modular converter topologies were presented based on a switched-capacitor cell concept in which a soft-switched scheme was used to reduce the switching loss and electromagnetic interference [8]. The coupled inductor-based converters are another solution to implement high step-up gain because the turns ratio of the coupled inductor can be employed as another control freedom to extend the voltage gain [9]. The converter achieves high step-up voltage gain with appropriate duty ratio and low voltage stress on the power switches. Also, the energy stored in the leakage inductor of the coupled inductor can be recycled to the output. However, the input current ripple is relatively larger by employing single-phase-coupled inductor-based converters, which may shorten the usage life of the input electrolytic capacitor.

In 2012 Wuhua Li et al proposed a paper on Interleaved High Step-Up Converter With Winding-Cross-Coupled Inductors and Voltage Multiplier Cells [10]. The voltage gain is extended and the switch voltage stress is reduced by the WCCIs and the voltage multiplier cells in the presented circuit, which minimizes the peak current ripple of the power devices and makes low-voltage MOSFETs with high performance available in high step-up and high output voltage applications. Moreover, the output diode reverse-recovery problem is alleviated by the leakage inductance of the WCCIs, which reduces the reverse-recovery losses. Alternatively, some interleaved high step-up converters with simplified coupled inductors are introduced to derive more compact circuit structure [11]. In 2007 Yungtaek Jang et al proposed an interleaved voltage doubler has been proposed for universal line power factor correction front end with automatic current sharing capability and lower active switch stress to increase the low-line efficiency [12]. The switching losses of the boost switches and reverse-recovery-related losses of boost rectifiers are also significantly reduced because in the voltage-doubler mode the switching voltages are reduced. To achieve higher voltage conversion ratio and further reduce voltage stress on the switch and diode, the high step-up ratio converter and the ultrahigh step-up converter have been proposed [13][14].

In this paper, a novel transformerless high voltage gain dc converter supplying single phase full bridge inverter is proposed. The proposed topology contains a converter section and an inverter section. The converter utilizes input parallel output series configuration for providing a much higher voltage gain without adopting an extreme large duty cycle. Closed loop PI controller is used to control the error and achieves the desired output voltage for the converter section. The converter section is followed by a single phase full bridge inverter. The inverter uses unipolar switching technique. Inverter offers reduced switching losses and generates less EMI. The inverter with filter circuit gives better output sinusoidal voltage.

The remaining contents of this paper may be outlined as follows. First, the novel circuit topology is given in Section 2. The operation principle of both converter and inverter are given in Section 3. Then, the corresponding steady state analysis is made in Section 4 to provide some basic converter and inverter characteristics. The simulation results are presented in Section 5. A prototype is then constructed some experimental results are then presented in Section 6 for demonstrating the merits and validity of the proposed converter. Finally, some conclusions are offered in the last section.

## **II. Proposed Topology**

The proposed topology consists of a converter section and an inverter section. The converter topology is basically derived from a two-phase interleaved boost converter and it utilizes input-parallel output-series configuration for providing much higher voltage gain without adopting extreme large duty cycle. Furthermore, the voltage stress of the active switches and diodes can be greatly reduced to enhance the overall conversion efficiency. The inverter section is a basic single phase full bridge inverter with unipolar switching. The unipolar switching inverter offers reduced switching losses and generates less EMI. Closed loop PI controller is used in the converter section to control the error and finally achieves the desired output voltage. The PI controller continuously calculates an error value as the difference between a measured process variable and a desired set point. The controller attempts to minimize error over time by adjustment of a control variable. PI controllers are fairly common, since derivative action is sensitive to measurement noise.

The inverter uses unipolar voltage switching. The unipolar modulation normally requires two sinusoidal modulating waves which are of same magnitude and frequency but  $180^\circ$  out of phase. Fig.1 shows the circuit configuration of the proposed topology. The diodes  $D_{1a}$ ,  $D_{2a}$  and capacitors  $C_a$ ,  $C_b$  are used to achieve high voltage gain in the converter section. During the energy transfer period, partial inductor stored energy is stored in one capacitor and partial inductor stored energy together with the other capacitor stored energy is transferred to the output to achieve much higher voltage gain. Furthermore, the converter possesses automatic uniform current sharing capability without adding extra circuitry or complex control methods. The resistors  $R_1$  and  $R_2$  are used to obtain the output voltage reference for the control circuit of the converter. Switches  $S_3$ ,  $S_4$ ,  $S_5$ ,

$S_6$  forms the single phase full bridge inverter. The unipolar switching technique is used for the inverter. In unipolar PWM, the desired voltage can be achieved by using a sequence of switching for each H-bridge inverter within short periods of time. Unipolar PWM can also be used for both lower and higher modulation indices. A low pass LC filter is used to obtain smooth sinusoidal waveform at the output.

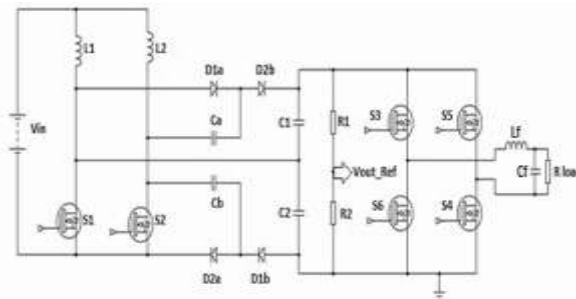


Fig.1.Circuit configuration of the proposed topology

### III. Operating Principle

#### 3.1. OPERATING PRINCIPLE OF THE CONVERTER SECTION

The main objective of the converter is to obtain high voltage gain and such characteristic can only be achieved when the duty cycle is greater than 0.5 and in continuous conduction mode (CCM). In order to simplify the circuit analysis of the proposed converter, some assumptions are made as follows:-

- 1) All components are ideal components.
- 2) The capacitors are sufficiently large, such that the voltages across them can be considered as constant approximately.
- 3) The system is under steady state and is operating in CCM and with duty ratio being greater than 0.5 for high step-up voltage purpose.

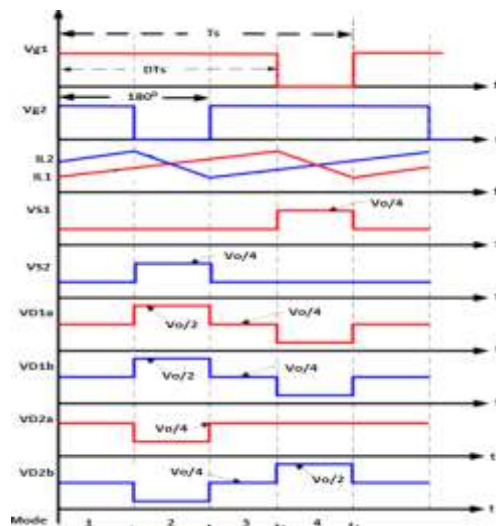


Fig.2.Key operating waveforms of the converter at CCM

Basically, the operating principle of the proposed converter can be classified into four operation modes. The interleaved gating signals with a 180° phase shift as well as some key operating waveforms are shown in Fig.2.

Mode 1 ( $t_0 \leq t < t_1$ ) :-

For mode 1, switches  $S_1$  and  $S_2$  are turned ON,  $D_{1a}$ ,  $D_{1b}$ ,  $D_{2a}$ ,  $D_{2b}$  are all OFF. The corresponding equivalent circuit is shown in Fig.3. From Fig.3, it is seen that both  $i_{L1}$  and  $i_{L2}$  are increasing to store energy in  $L_1$  and  $L_2$  respectively. The voltages across diodes  $D_{1a}$  and  $D_{2a}$  are clamped to capacitor voltage  $v_{Ca}$  and  $v_{Cb}$  respectively, and the voltages across the diodes  $D_{1b}$  and  $D_{2b}$  are clamped to  $v_{C2}$  minus  $v_{Cb}$  and  $v_{C1}$  minus  $v_{Ca}$  respectively. Also, the load power is supplied from capacitors  $C_1$  and  $C_2$ .

The corresponding state equations are given as follows:-

$$L_1 \frac{di_{L1}}{dt} = V_{in} \dots\dots\dots (1)$$

$$L_2 \frac{di_{L2}}{dt} = V_{in} \dots\dots\dots (2)$$

$$C_a \frac{dv_{Ca}}{dt} = 0 \dots\dots\dots (3)$$

$$C_b \frac{dv_{Cb}}{dt} = 0 \dots\dots\dots (4)$$

$$C_1 \frac{dv_{C1}}{dt} = - \frac{(v_{C1} + v_{C2})}{R} \dots\dots\dots (5)$$

$$C_2 \frac{dv_{C2}}{dt} = - \frac{(v_{C1} + v_{C2})}{R} \dots\dots\dots (6)$$

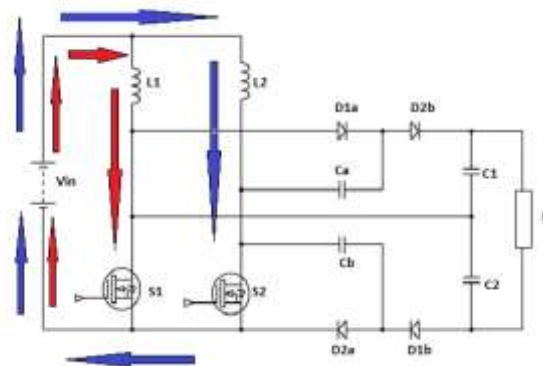


Fig.3.Equivalent circuit of the converter in mode 1 and mode 3 operation

Mode 2 ( $t_1 \leq t < t_2$ ) :-

For this operation mode, switch  $S_1$  remains conducting and  $S_2$  is turned OFF. Diodes  $D_{2a}$  and  $D_{2b}$  become conducting. The corresponding equivalent circuit is shown in Fig.4. It is seen from Fig.4, that part of stored energy in inductor  $L_2$  as well as the stored energy of  $C_a$  is now released to output capacitor  $C_1$  and load. Meanwhile, part of stored energy in inductor  $L_2$  is stored in  $C_b$ . In this mode, capacitor voltage  $v_{C1}$  is equal to  $v_{Cb}$  plus  $v_{Ca}$ . Thus,  $i_{L1}$  still increases continuously and  $i_{L2}$  decreases linearly.

The corresponding state equations are given as follows:-

$$L_1 \frac{di_{L1}}{dt} = V_{in} \dots\dots\dots (7)$$

$$L_2 \frac{di_{L2}}{dt} = V_{in} + v_{Ca} - v_{C1} = V_{in} - v_{Cb} \dots\dots\dots (8)$$

$$C_a \frac{dv_{Ca}}{dt} = i_{Cb} - i_{L2} \dots\dots\dots (9)$$

$$C_b \frac{dv_{Cb}}{dt} = i_{Ca} + i_{L2} \dots\dots\dots (10)$$

$$C_1 \frac{dv_{C1}}{dt} = -i_{Ca} - \frac{(v_{C1} + v_{C2})}{R} \dots\dots\dots (11)$$

$$C_2 \frac{dv_{C2}}{dt} = - \frac{(v_{C1} + v_{C2})}{R} \dots\dots\dots (12)$$

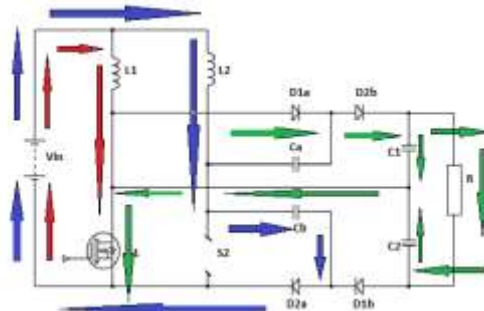


Fig.4.Equivalent circuit of the converter in mode 2 operation

Mode 3 ( $t_2 \leq t < t_3$ ) :-

For this operation mode, as can be observed from Fig.3, both  $S_1$  and  $S_2$  are turned ON. The corresponding equivalent circuit turns out to be the same as Fig.3.

Mode 4 ( $t_3 \leq t < t_4$ ) :-

For this operation mode, switch  $S_2$  remains conducting and  $S_1$  is turned OFF. Diodes  $D_{1a}$  and  $D_{1b}$  become conducting. The corresponding equivalent circuit is shown in Fig.5.

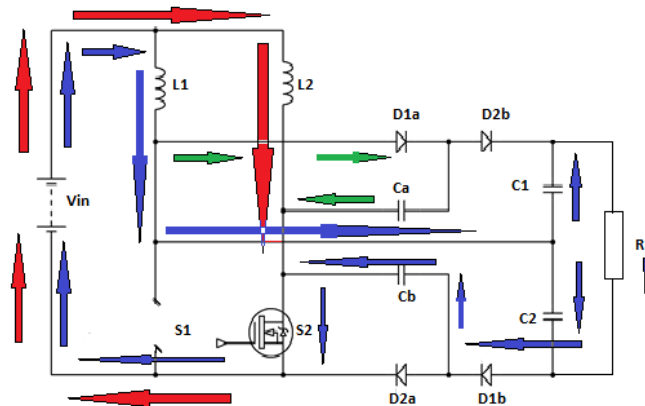


Fig.5.Equivalent circuit of the converter in mode 4 operation

It is seen from Fig.5, that the part of stored energy in inductor  $L_1$  as well as the stored energy of  $C_b$  is now released to output capacitor  $C_2$  and load. Meanwhile, part of stored energy in inductor  $L_1$  is stored in  $C_a$ . In this mode, the output capacitor voltage  $v_{C2}$  is equal to  $v_{Cb}$  plus  $v_{Ca}$ . Thus,  $i_{L2}$  still increases continuously and  $i_{L1}$  decreases linearly.

The corresponding state equations are given as follows:-

$$L_1 \frac{di_{L1}}{dt} = V_{in} - v_{C2} + v_{Cb} = V_{in} - v_{Ca} \dots\dots\dots (13)$$

$$L_2 \frac{di_{L2}}{dt} = V_{in} \dots\dots\dots (14)$$

$$C_a \frac{dv_{Ca}}{dt} = i_{Cb} + i_{L1} \dots\dots\dots (15)$$

$$C_b \frac{dv_{Cb}}{dt} = i_{Ca} - i_{L1} \dots\dots\dots (16)$$

$$C_1 \frac{dv_{C1}}{dt} = - \frac{(v_{C1} + v_{C2})}{R} \dots\dots\dots (17)$$

$$C_2 \frac{dv_{C2}}{dt} = -i_{Cb} - \frac{(v_{C1} + v_{C2})}{R} \dots\dots\dots (18)$$

From the above illustration of the proposed converter, one can see that the operations of two-phase are both symmetric and rather easy to implement. Also, from key operating waveforms of the proposed converter is shown in Fig.2. One can see the low voltage stress of two active switches and four diodes as well as the uniform current sharing.

### 3.2. Operating Principle Of The Inverter Section

The inverter circuit performs the task of converting DC input power to AC output power. The proposed topology uses a single phase full bridge inverter with unipolar switching. The full bridge inverter has two legs consisting of two semiconductor switches in each of them with the load connected at the center points of the two legs.

Fig.6 shows the unipolar single phase full bridge inverter with low pass LC filter. As seen in Fig.6 four semiconductor switches  $S_3, S_4, S_5, S_6$  are arranged with the load connected at the midpoints of the two legs, hence forming the letter H, so the name H-Bridge inverter. DC voltage  $V_{dc}$  is supplied to H-Bridge. The switches  $S_3, S_4, S_5, S_6$  can be switched in three different sequences :-

- 1) When  $S_3$  and  $S_4$  are turned on  $+V_{dc}$  is obtained at the output
- 2) When  $S_5$  and  $S_6$  are turned on  $-V_{dc}$  is obtained at the output
- 3) When  $S_3$  and  $S_5$  or  $S_6$  and  $S_4$  are turned on together zero voltage is obtained at the output

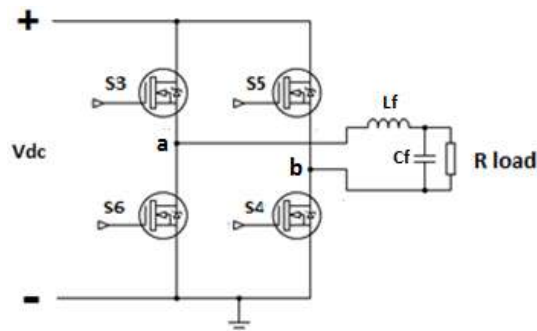


Fig.6.unipolar single phase full bridge inverter

The unipolar modulation normally requires two sinusoidal modulating waves which are of same magnitude and frequency but  $180^\circ$  out of phase. The two modulating wave are compared with a common triangular carrier wave generating two gating signals for the upper two switches  $S_3$  and  $S_5$ . The upper and the lower switches in the same inverter leg work in a complementary manner with one switch turned on and other turned off. Thus we need to consider only two independent gating signals  $V_{g3}$  and  $V_{g5}$  which are generated by comparing sinusoidal modulating wave  $V_{sine}$  and triangular carrier wave  $V_{tri}$ . The inverter terminal voltages are obtained denoted by  $V_{an}$  and  $V_{bn}$  and the inverter output voltage is given by,

$$\text{Inverter output voltage, } V_{ab} = V_{an} - V_{bn} \dots\dots (19)$$

The inverter output voltage switches between either between zero and  $+V_{dc}$  during positive half cycle or between zero and  $-V_{dc}$  during negative half cycle of the fundamental frequency thus this scheme is called unipolar modulation. The unipolar switched inverter offers reduced switching losses and generates less EMI. On efficiency grounds, it appears that the unipolar switched inverter has an advantage.

Table.1.Unipolar switching algorithm

Switches [On]	Unipolar Switching Logarithm
S3	$V_{sine} \geq V_{tri}$ , then $V_{an} = V_{dc}$
S6	$V_{sine} < V_{tri}$ , then $V_{an} = 0$
S5	$-V_{sine} \geq V_{tri}$ , then $V_{bn} = V_{dc}$
S4	$-V_{sine} < V_{tri}$ , then $V_{bn} = 0$

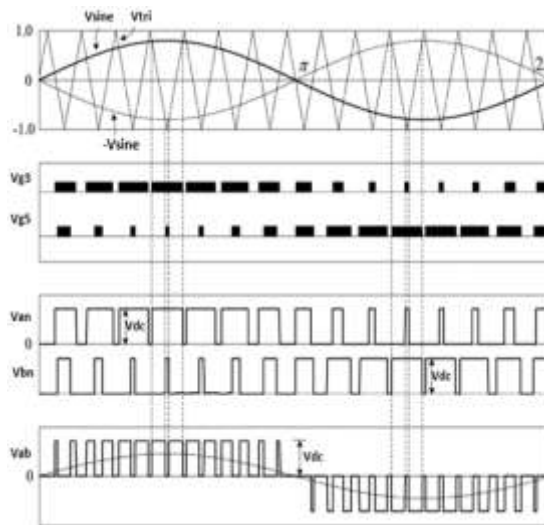


Fig.7. Waveforms of unipolar switching scheme

The output voltage of unipolar single phase full bridge inverter is given by,

$$V_o = m_a * V_{dc} * \sin(\omega t) \dots \dots \dots (20)$$

$$m_a = \frac{\text{peak of control signal (sine wave)}}{\text{peak of triangular wave}} ; 0 \leq m_a \leq 1$$

This voltage can be filtered using a LC low-pass filter. The voltage on the output of the filter will closely resemble the shape and frequency of the modulation signal. This means that the frequency, wave-shape, and amplitude of the inverter output voltage can all be controlled as long as the switching frequency is at least 25 to 100 times higher than the fundamental output frequency of the inverter. The actual generation of the PWM signals is mostly done using microcontrollers and digital signal processors.

#### IV. Steady State Analysis

##### 4.1. Steady State Analysis Of The Converter Section

##### 4.1.1. Voltage Gain

Referring to Fig.3 and 5, from the volt-second relationship of inductor  $L_1$  (or  $L_2$ ), one can obtain the following relations :-

$$V_{in} D + (V_{in} - V_{Ca})(1 - D) = 0 \dots \dots \dots (21)$$

$$V_{in} D + (V_{in} - V_{Cb})(1 - D) = 0 \dots \dots \dots (22)$$

Also from the equivalent circuits in Fig.4 and 5 voltage  $V_{C1}$  and  $V_{C2}$  can be derived as follows by substituting the  $V_{Ca}$  and  $V_{Cb}$  solutions of (21) and (22) :-

$$V_{C1} = V_{Ca} + V_{Cb} = \frac{2}{1-D} V_{in} \dots \dots \dots (23)$$

$$V_{C2} = V_{Ca} + V_{Cb} = \frac{2}{1-D} V_{in} \dots \dots \dots (24)$$

It follows from (23) and (24) that the output voltage can be obtained as follows :-

$$V_o = V_{C1} + V_{C2} = \frac{4}{1-D} V_{in} \dots\dots\dots (25)$$

Thus, the voltage conversion ratio M of the converter can be obtained as follows :-

$$M = \frac{V_o}{V_{in}} = \frac{4}{1-D} \dots\dots\dots (26)$$

#### 4.1.2. Voltage stresses on semiconductor devices

To simplify the voltage stress analysis of the components of the proposed converter, the voltage ripples on the capacitors are ignored. From Fig.4 and 5, one can see that the voltage stresses on active power switches S<sub>1</sub> and S<sub>2</sub> can be obtained directly as shown in the following equation :-

$$V_{S1,max} = V_{S2,max} = \frac{1}{1-D} V_{in} \dots\dots\dots (27)$$

Substituting (25) into (27), the voltage stresses on the active power switches can be expressed as,

$$V_{S1,max} = V_{S2,max} = \frac{V_o}{4} \dots\dots\dots (28)$$

From (28), one can see that the voltage stress of active switches of the proposed converter is equal to one fourth of the output voltage. Hence, the converter enables one to adopt lower voltage rating devices to further reduce both switching and conduction losses. As can be observed from the equivalent circuits in 3 and 4, the open circuit voltage stress of diodes D<sub>1a</sub>, D<sub>2a</sub>, D<sub>1b</sub> and D<sub>2b</sub> can be obtained directly as shown in (29).

$$V_{D1a,max} = V_{D1b,max} = V_{D2b,max} = \frac{V_o}{2}; V_{D2a,max} = \frac{V_o}{4} \dots\dots\dots (29)$$

In fact, one can see from (29) that the maximum resulting voltage stress of diodes is equal to V<sub>o</sub>/2. Hence, the converter enables one to adopt lower voltage rating diodes to further reduce conduction losses. This paper presents closed loop control of the converter. The closed loop control of the converter is achieved by using processor such as dsPIC30F2010.

#### 4.1.3. Characteristic of uniform current input inductor current sharing

By using the state space averaging technique, one can repeat the previous process to get the averaged state equations quite straightforward as follows:-

$$L_1 \frac{di_{L1}}{dt} = V_{in} - (1-D)V_{Ca} \dots\dots\dots (30)$$

$$L_2 \frac{di_{L2}}{dt} = V_{in} - (1-D)V_{Cb} \dots\dots\dots (31)$$

$$C_a \frac{dv_{Ca}}{dt} = \frac{(1-D)C_a (C_{eq1} I_{L1}(C_2+C_b) - C_{eq2} I_{L2} C_1)}{C_{eq1} C_{eq2}} - \frac{(1-D)C_a C_b (C_{eq1} + C_{eq2})(V_{C1} + V_{C2})}{C_{eq1} C_{eq2} R} \dots\dots\dots (32)$$

$$C_b \frac{dv_{Cb}}{dt} = \frac{(1-D)C_b (C_{eq2} I_{L2}(C_1+C_a) - C_{eq1} I_{L1} C_2)}{C_{eq1} C_{eq2}} - \frac{(1-D)C_a C_b (C_{eq1} + C_{eq2})(V_{C1} + V_{C2})}{C_{eq1} C_{eq2} R} \dots\dots\dots (33)$$

$$C_1 \frac{dv_{C1}}{dt} = \frac{(1-D)C_a (C_a I_{L2} R - (C_a + C_b)(V_{C1} + V_{C2}))}{C_{eq1} R} - \frac{D(V_{C1} + V_{C2})}{R} \dots\dots\dots (34)$$

$$C_2 \frac{dv_{C2}}{dt} = \frac{(1-D)C_2 (C_b I_{L1} R - (C_a + C_b)(V_{C1} + V_{C2}))}{C_{eq2} R} - \frac{D(V_{C1} + V_{C2})}{R} \dots\dots\dots (35)$$

Where i<sub>L1</sub>, i<sub>L2</sub>, v<sub>Ca</sub>, v<sub>Cb</sub>, v<sub>C1</sub> and v<sub>C2</sub> denote the average state variables. I<sub>L1</sub>, I<sub>L2</sub>, V<sub>Ca</sub>, V<sub>Cb</sub>, V<sub>C1</sub> and V<sub>C2</sub> represent the corresponding dc values. C<sub>eq1</sub> = C<sub>1</sub>C<sub>a</sub> + C<sub>1</sub>C<sub>b</sub> + C<sub>a</sub>C<sub>b</sub>, C<sub>eq2</sub> = C<sub>2</sub>C<sub>a</sub> + C<sub>2</sub>C<sub>b</sub> + C<sub>a</sub>C<sub>b</sub> and I<sub>o</sub> =  $\frac{(V_{C1} + V_{C2})}{R}$ .

By selecting C<sub>1</sub> = C<sub>2</sub> = C<sub>x</sub>, C<sub>a</sub> = C<sub>b</sub> = C<sub>y</sub>, one can get the corresponding dc solutions as follows :-



$$I_{L1} = I_{L2} = \left[ \frac{2}{1-D} + \frac{DC_y}{(1-D)C_x} \right] I_o \dots\dots\dots (36)$$

From (36), one can see that the converter indeed possesses the inherent automatic uniform current sharing capability.

#### 4.2. STEADY STATE ANALYSIS OF THE INVERTER SECTION

For a single phase full bridge inverter, the load voltage waveform does not depend on the nature of load. The load voltage is given by,

$$v_o = V_{dc} ; \text{ For } 0 < t < T/2 \dots\dots\dots (37)$$

$$v_o = -V_{dc} ; \text{ For } T/2 < t < T \dots\dots\dots (38)$$

The load current is, however, dependent upon the nature of load. Let the load in general, consists of RLC in series. The circuit model of single phase full bridge inverter is shown in Fig.8. In this circuit, load current would finally settle down to steady state conditions and would vary periodically.

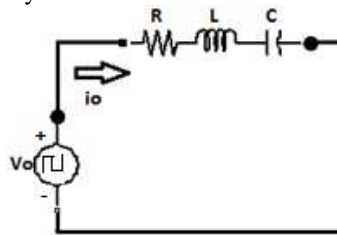


Fig.8.Circuit model of single phase full bridge inverter

The voltage equation for the circuit model for  $0 < t < T/2$  is given by,

$$V_{dc} = Ri_o + L \frac{di_o}{dt} + \frac{1}{C} \int i_o dt + V_{C1} \dots\dots\dots (39)$$

For  $T/2 < t < T$  or  $0 < t' < T/2$ , the voltage equation is given by,

$$-V_{dc} = Ri_o + L \frac{di_o}{dt'} + \frac{1}{C} \int i_o dt' + V_{C2} \dots\dots\dots (40)$$

$V_{C1}$  : initial voltage across the capacitor at  $t = 0$   
 $V_{C2}$  : initial voltage across the capacitor at  $t' = 0$

Differentiating equations (39) and (40) gives,

$$\frac{d^2i_o}{dt^2} + \frac{R}{L} \frac{di_o}{dt} + \frac{1}{LC} i_o = 0 \dots\dots\dots (41)$$

$$\frac{d^2i_o}{dt'^2} + \frac{R}{L} \frac{di_o}{dt'} + \frac{1}{LC} i_o = 0 \dots\dots\dots (42)$$

The solution of these second order equations can be obtained by using initial conditions as specified above. Components constituting the load decide the nature of load current waveforms. For R load, load current waveform  $i_o$  is identical with the load voltage waveform  $v_o$ .

### V. Simulation Results

The proposed topology is simulated by using MATLAB (Simulink) software. For simulation 25V dc input, 320V(peak) ac output model of the proposed topology is considered. The switching frequency of the converter and inverter are chosen to be 40KHz and 1KHz respectively. The duty ratios of switches  $S_1$  and  $S_2$  equal to 0.75. The boost inductors  $L_1, L_2$  takes the value 253 $\mu$ H. The blocking capacitors  $C_a, C_b$  are chosen to be

10 $\mu$ F. The value of capacitors  $C_1$  and  $C_2$  is equal to 250 $\mu$ F. The L and C values of the filter circuit are 10.13H and 1 $\mu$ F respectively. The load value is set to 3500 $\Omega$ . Fig.9 shows the MATLAB Simulink model of the proposed topology. The simulation waveforms of the switching pulses to the converter and inverter are shown in Fig.10 and Fig.11 respectively. The duty ratios of both the switches of the converter,  $S_1$  and  $S_2$  are chosen to be 0.75 for continuous conduction mode of operation. The switching pulses for converter switches are given with a phase shift of 180 $^\circ$ . The inverter uses unipolar voltage switching scheme.

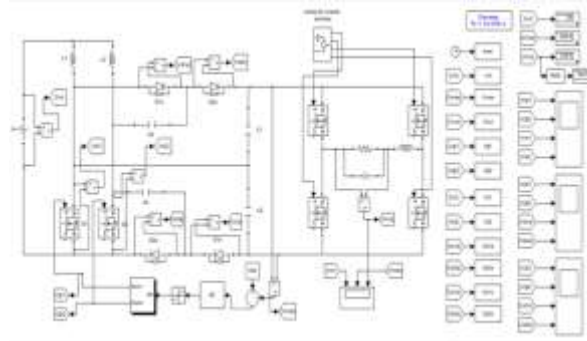


Fig.9.MATLAB Simulink model of the proposed topology

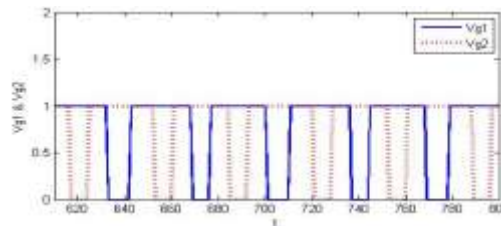


Fig.10.Switching pulses to the converter switches  $S_1$  and  $S_2$

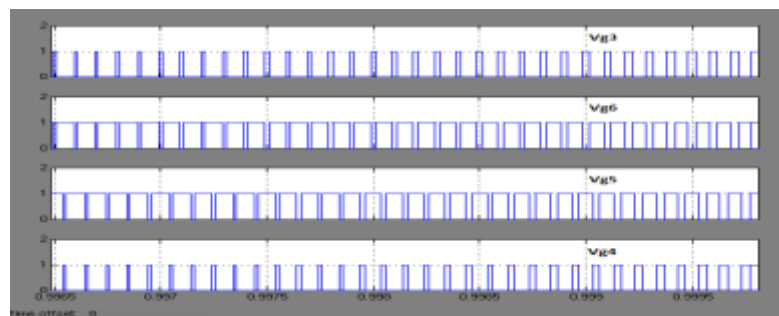


Fig.11.Switching pulses to the inverter switches  $S_3, S_6, S_5, S_4$

The simulation waveforms of the input voltage, intermediate voltage (converter output voltage) and output voltage are shown in Fig.12. The measured input voltage is 25V. The intermediate voltage and the output voltage are 400V and 320V(peak) from fig.12.

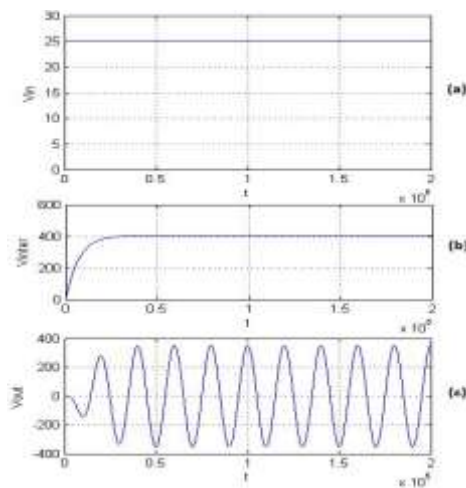


Fig.12.Simulation waveforms of (a) input voltage (b) intermediate voltage (c) output voltage

To check the validity of the capacitor voltage stress, waveforms of voltage across blocking capacitors and capacitors  $C_1$ ,  $C_2$  are recorded as shown in Fig.13. From Fig.13, one can see that the voltage stresses of the capacitor  $C_1$ ,  $C_2$  and blocking capacitors  $C_a$ ,  $C_b$  are indeed equal to one half and one fourth of the output voltage respectively. when the converter is operated in modes 2 and 4, the voltages of capacitors  $C_a$  and  $C_b$  are clamped at  $V_{in}/(1-D)$  and when converter is operated in modes 1 and 3, all diodes are OFF, and capacitors  $C_a$  and  $C_b$  are isolated as open circuits, hence the voltages of capacitors  $C_a$  and  $C_b$  are kept constant. Also, the output loading is mainly supplied by capacitors  $C_1$  and  $C_2$ .

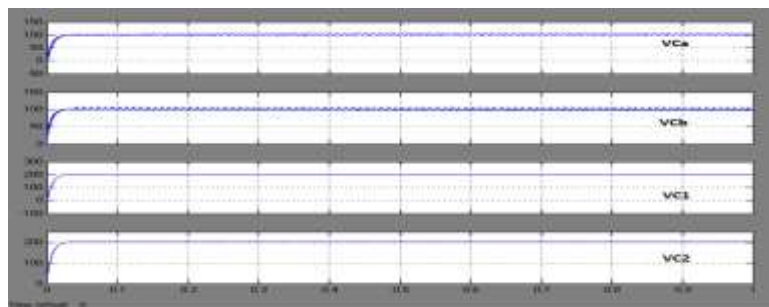
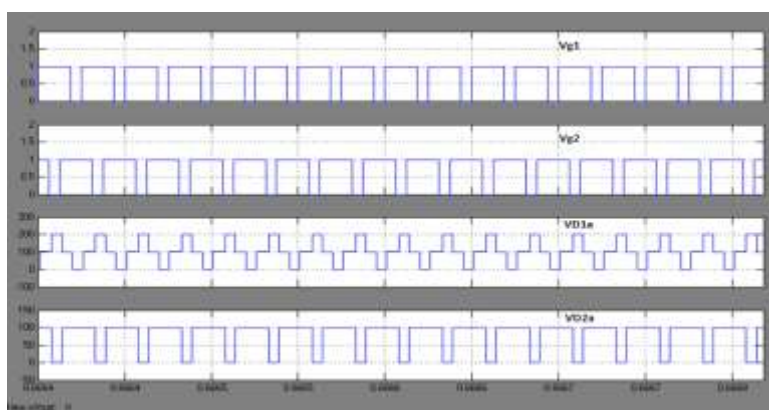


Fig.13.Simulation waveforms of the blocking capacitors ( $C_a, C_b$ ) and capacitors  $C_1, C_2$  voltages

The diode voltage waveforms of the simulation results are shown in Fig.14 and Fig.15, which indicates that the maximum voltage cross diodes  $V_{D1a}$ ,  $V_{D1b}$ , and  $V_{D2b}$  equals 200V which is indeed equal to one-half of the output voltage. The maximum voltage crosses diode  $V_{D2a}$  is 100 V which is equal to one fourth of the output voltage as expected.





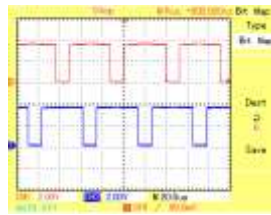


Fig.18.Switching pulses to the converter

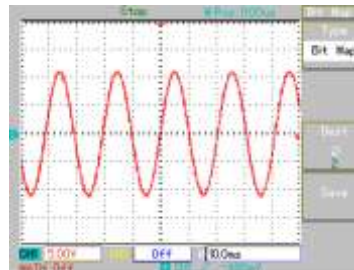


Fig.19.Output ac voltage of the proposed converter (probe is set at 10X)

Fig.19 shows the output ac voltage of the proposed topology. The measured input voltage is 12V and the output voltage is measured to be 100V.

Table.2.Components and its specification

COMPONENTS	SPECIFICATION
Boost Inductors (L1, L2)	0.3mH
Active switches of converter (S1, S2)	IRF840
Blocking capacitors (Ca, Cb)	10 $\mu$ F
Capacitors C1, C2	1000 $\mu$ F
Power diodes (D1a, D2a, D1b, D2b)	HF064
Active Switches of inverter (S3, S4, S5, S6)	P60
Filter inductor (Lf)	10.13 $\mu$ H
Filter Capacitor (Cf)	1 $\mu$ F
Load (R)	1500 $\Omega$

## VII. CONCLUSION

In this paper, a novel transformerless DC converter supplying single phase full bridge inverter is proposed. The proposed topology contains a transformerless dc converter followed by a single phase full bridge inverter. The proposed topology possesses high voltage gain and reduced switching losses. The converter features automatic current sharing characteristic. The converter output is controlled by using a PI controller. The inverter uses unipolar switching scheme and which offers reduced switching losses and generates less EMI. Both the inverter and converter controls are implemented using DSPIC30F2010. The proposed topology can be used in UPS, power grid and renewable energy applications.

## References

- [1] Ching-Tsai Pan, Chen-Feng Chuang, and Chia-Chi Chu "A Novel Transformer-less Adaptable Voltage Quadrupler DC Converter with Low Switch Voltage Stress" IEEE Transactions On Power Electronics, Vol. 29, No. 9, September 2014
- [2] W. Li and X. He, "Review of non-isolated high step-up DC/DC converters in photovoltaic grid-connected applications," IEEE Trans. Ind. Electron., vol. 58, no. 4, pp. 1239–1250, Apr. 2011.
- [3] C. M. Wang, "A novel ZCS-PWM flyback converter with a simple ZCS PWM commutation cell," IEEE Trans. Ind. Electron., vol. 55, no. 2, pp. 749–757, Feb. 2008.
- [4] J. M. Kwon and B. H. Kwon, "High step-up active-clamp converter with input-current doubler and output-voltage doubler for fuel cell power systems," IEEE Trans. Power Electron., vol. 24, no. 1, pp. 108–115, Jan. 2009.
- [5] R. J. Wai, W. H. Wang, and C. Y. Lin, "High-performance stand-alone photovoltaic generation system," IEEE Trans. Ind. Electron., vol. 55, no. 1, pp. 240–250, Jan. 2008.

- [6] M. Prudente, L. L. Pfitscher, G. Emmendoerfer, E. F. Romaneli, and R. Gules, "Voltage multiplier cells applied to non-isolated DC–DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 871–887, Mar. 2008.
- [7] C. Chun-Kit, T. Siew-Chong, C. K. Tse, and A. Ioinovici, "On energy efficiency of switched capacitor converters," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 862–876, Feb. 2013.
- [8] Z. Ke, M. J. Scott, and W. Jin, "Switched-Capacitor-Cell-Based voltage multipliers and DC–AC inverters," *IEEE Trans. Ind. Appl.*, vol. 48, no. 5, pp. 1598–1609, Sep./Oct. 2012.
- [9] L. S. Yang, T. J. Liang, H. C. Lee, and J. F. Chen, "Novel high step-up DC–DC converter with coupled-inductor and voltage-doubler circuits," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4196–4206, Sep. 2011.
- [10] W. Li, Y. Zhao, J. Wu, and X. He, "Interleaved high step-up converter with winding-cross-coupled inductors and voltage multiplier cells," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 133–143, Jan. 2012.
- [11] G. A. L. Henn, R. N. A. L. Silva, P. P. Praca, L. H. S. C. Barreto, and D. S. Oliveira, Jr., "Interleaved-boost converter with high voltage gain," *IEEE Trans. Power Electron.*, vol. 25, no. 11, pp. 2753–2761, Nov. 2010.
- [12] Y. T. Jang and M. M. Jovanovic, "Interleaved boost converter with intrinsic voltage-doubler characteristic for universal-line PFC front end," *IEEE Trans. on Power Electron.*, vol. 22, no. 4, pp. 1394–1401, Jul. 2007.
- [13] L. S. Yang, T. J. Liang, and J. F. Chen, "Transformerless DC–DC converters with high step-up voltage gain," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 3144–3152, Aug. 2009.
- [14] A. A. Fardoun and E. H. Ismail, "Ultra step-up DC–DC converters with reduced switch stress," *IEEE Trans. Ind. Appl.*, vol. 46, no. 5, pp. 2025–2034, Oct. 2010.
- [15] W. Li, Y. Zhao, Y. Deng, and X. He, "Interleaved converter with voltage multiplier cell for high step-up and high efficiency conversion," *IEEE Trans. Power Electron.*, vol. 25, no. 9, pp. 2397–2408, Sep. 2010.
- [16] C. M. Lai, C. T. Pan, and M. C. Cheng, "High-efficiency modular high step-up interleaved boost converter for DC-microgrid applications," *IEEE Trans. Ind. Electron.*, vol. 48, no. 1, pp. 161–171, Jan./Feb. 2012.